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ISSUE CLASSIFICATION	
Class	Subclass

PATENT NUMBER

U.S. UTILITY Patent Application

<p>O.I.P.E.</p> <p>17CJL CHH</p> <p>SCANNED Q.A.</p>	<p>PATENT DATE</p>
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CLASS	APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
	09/591621		703	14	2763 2123	Rosales-Ho CHOT

[illegible]

Vidvabhusan Gupta

System and method for designing and optimizing the memory of an embedded processing system

PTO-2040
12/99[illegible]

<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS		CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims
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